

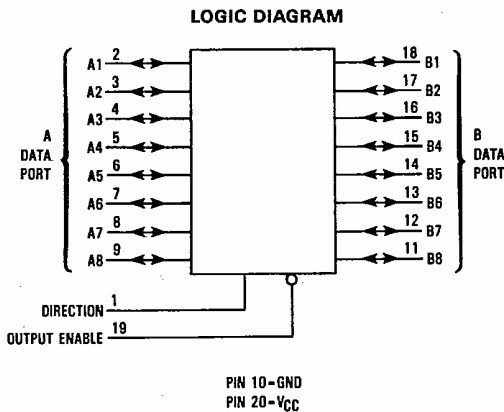
Advance Information
Octal 3-State Noninverting Bus Transceiver
High-Performance Silicon-Gate CMOS

The MC54/74HC245A is identical in pinout to the LS245. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

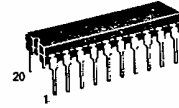
The HC245A is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The MC245A performs functions similar to those of the HC640A and the HC643A.

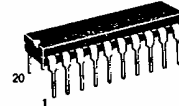
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 308 FETs or 77 Equivalent Gates



MC54/74HC245A



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-02



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74HCXXXAN Plastic
 MC54HCXXXAJ Ceramic
 MC74HCXXXADW SOIC

$T_A = -55^\circ$ to 125°C for all packages.

PIN ASSIGNMENT

DIRECTION	1	20	VCC
A1	2	19	OUTPUT ENABLE
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High-Impedance State)

X = don't care

MC54/74HC245A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{I/O}	DC I/O Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin 1 or 19	±20	mA
I _{I/O}	DC I/O Current, per I/O Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	-55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} =2.0 V V _{CC} =4.5 V V _{CC} =6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	V	
			4.5	3.15	3.15		
			6.0	4.2	4.2		
V _{IL}	Maximum Low-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	V	
			4.5	0.9	0.9		
			6.0	1.2	1.2		
V _{OH}	Minimum High-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	V	
			4.5	4.4	4.4		
			6.0	5.9	5.9		
V _{OL}	Maximum Low-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	V	
			4.5	0.1	0.1		
			6.0	0.1	0.1		
		V _{in} =V _{IH} or V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5	3.98	3.84		
			6.0	5.48	5.34		
			6.0	0.26	0.33		0.40
I _{in}	Maximum Input Leakage Current	V _{in} =V _{CC} or GND, Pin 1 or 19	6.0	±0.1	±1.0	μA	
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} =V _{IL} or V _{IH} V _{out} =V _{CC} or GND, I/O Pins	6.0	±0.5	±5.0	μA	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} =V _{CC} or GND I _{out} =0 μA	6.0	4	40	μA	

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 4, of the Motorola High-Speed CMOS Logic Data Book — DL129/R3.

MC54/74HC245A

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
tPLH, tPHL	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
tPLZ, tPHZ	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
tpZL, tpZH	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance (Pin 1 or Pin 19)	—	10	10	10	pF
C _{out}	Maximum Three-State I/O Capacitance (I/O in High-Impedance State)	—	15	15	15	pF

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, VCC = 5.0 V	
		40	pF

NOTE: For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4, of the Motorola High-Speed CMOS Logic Data Book — DL129/R3.

SWITCHING WAVEFORMS

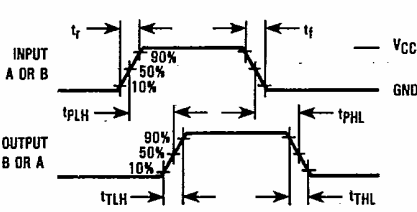


Figure 1

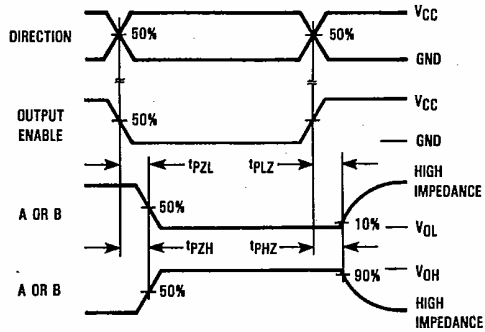
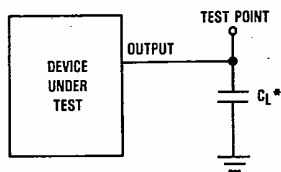
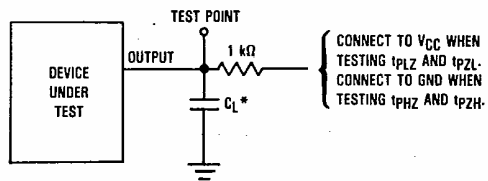


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

MC54/74HC245A

EXPANDED LOGIC DIAGRAM

